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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/350,436	07/09/1999	CHANG-RAE JEONG	P992004	8102

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EXAMINER	
WANG, TED M	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 08/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/350,436	JEONG, CHANG-RAE	
	Examiner	Art Unit	
	Ted M. Wang	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6 and 9-11* is/are rejected.

7)☒ Claim(s) *3,7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed on 05/22/2006, have been fully considered but they are not persuasive. The Examiner has thoroughly reviewed Applicants' arguments but firmly believes that the cited reference to reasonably and properly meet the claimed limitations.

Independent Claims 1 and 6

(1) *Applicants' argument* – "Takahashi teaches that the memory 24, as does the prior art disclosed in the present application, converts the modulation of the signal contained in ALL channels, indiscriminately (id.). The Applicant, with utmost respect, submits that the statement by Takahasili cited in the Office Action, at page 4, line 4-7, does not support the rejections. ... Therefore, the applicant respectfully submits that Takahashi does not disclose a "codec means for selectively converting said identified input digital signals received in said at least one channel from the first modulation standard to the second modulation standard in response to said channel select signal." as recited in claims 1 and 6."

Examiner's response –

In response to applicant's argument as recited in the above paragraph, the Takahashi's reference, Fig.3, column 3 lines 41-65 and Tables 1 and 2, teaches that the ROM 24 is addressed in part by bits B2-B8 of an 7 bit PCM signal output by the secondary time switch 23 during each time slot. The bits B2-B8 form bits A0-A6 of a partial address in the encoding law conversion memory 24. The

Tables 1 and 2 indicate the relationship between decoder output value number and the corresponding 7 bits (B2-B8) signal under A-law and μ-law encoding, respectively. The values indicated in Tables 1 and 2 are from CCITT Recommendation G.711 Table 1a and 2a. Table 1 indicates that the PCM channels (Channel No.1 –128) are represented by the combination bit values of B2-B8 (Fig.3 element 24 input address line B2-B7/A6-A0), respectively, for A-law input. Table 2 indicates that the PCM channels (Channel No.0 –127) are one-to-one corresponding to the combination bit values of B2-B8 (Fig.3 element 24 input address line B2-B7/A6-A0), respectively, for μ-law input. Now, returning back to Fig.3, at any instant period of time, there is only one PCM channel being selected and identified with respect to the particular B2-B7 values shown in Table 1 or 2 along with the control bits, P, M1, M0, C2, C1 and C0, and being converted from one of two different modulation standard (A-law or μ-law) to the other one of the two modulation standards (μ-law or A-law). Therefore, it is clear that Takahashi teaches a channel selector (Fig.2 element 23, Fig.3 signal B8-B2, A6-A0, column 3 lines 44-50) for generating a channel select signal (Fig.3 signal B8-B2) for identifying one of said plurality of communication channels (Tables 1 and 2) in said system.

Thus, for the explanation addressed in the above paragraph, the rejection under 35 U.S.C. 103(a) with Takahashi reference is adequate.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 9 recites the limitation "a third buffer" and "a fourth buffer" in line 3 and 4, respectively. There is insufficient antecedent basis for this limitation in the claim.

- With regard claim 9, the limitation "a third buffer" and "a fourth buffer" in line 3 and 4, respectively, as recited is unclear since – first buffer -- and – second buffer --, have not been introduced previously. The claim 8 and 9 are in different claim trees that are not related each other. A third and fourth buffers without introducing the first and second buffers make the claim 9 indefinite that there is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 4-6,10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi (US 4,661,946) in view of Eagan et al. (US 5,303,191).

- With regard claim 1, Takahashi discloses a digital switch module having encoding law conversion capability for converting pulse code modulation (PCM) signals (column 1 lines 45-63, and column 3 lines 56-65) from either one of two different modulation standards to the other one of said two different modulation

standards (Fig.1 elements 13 and 14) in a system characterized by having a plurality of communication channels with each channel having a plurality of input digital signals modulated by said one of said two different modulation standards (column 2 line 62 – column 3 line 19 and Fig.1 elements 10, 13, and 14) that comprise:

a channel selector (Fig.2 element 23, Fig.3 signal B8-B2, A6-A0, column 3 lines 44-50) for generating a channel select signal (Fig.3 signal B8-B2) for identifying one of said plurality of communication channels (Tables 1 and 2) in said system;

at least one codec (Fig.1-4 element 24) means for selectively converting said identified input digital signals received in said one of said plurality of communication channels channel (Fig.3 signal B8-B2 and Tables 1 and 2) from said one of said two different modulation standards to the other one of said two different modulation standards in response to said channel select signal (Fig.3 control bits M1 and M0, Table 3, column 5 lines 8-51),

a plurality of output voice/data signals, being converted/ driven by encoding conversion memory 24, have been selectively released and transmitted (column 3 line 7- column 5 line 51) said input digital signal (Fig. 1-4 elements 24 and column 3 line 7 – column 6 line 39) modulated by said one of said two different modulation standards (Fig.1 elements 10, 13, and 14 and column 2 line 62 – column 3 line 19) and said converted input digital signal to the other one of said two different modulation standards by said codec means in response to said

channel select signal (Fig. 1-4 elements 24 and 29, and column 2 line 62 – column 3 line 40, column 3 line 41 – column 5 line 51, and column 6 lines 1-46) by the control memory 29.

In Fig.3, column 3 lines 41-65, and Tables 1 and 2, Takahashi teaches that the ROM 24 is addressed in part by bits B2-B8 of an 7 bit PCM signal output by the secondary time switch 23 during each time slot. The bits B2-B8 form bits A0-A6 of a partial address in the encoding law conversion memory 24. The Tables 1 and 2 indicate the relationship between decoder output value number and the corresponding 7 bits (B2-B8) signal under A-law and μ-law encoding, respectively. The values indicated in Tables 1 and 2 are from CCITT Recommendation G.711 Table 1a and 2a. Table 1 indicates that the PCM channels (Channel No.1 –128) are represented by the combination bit values of B2-B8 (Fig.3 element 24 input address line B2-B7/A6-A0), respectively, for A-law input. Table 2 indicates that the PCM channels (Channel No.0 –127) are one-to-one corresponding to the combination bit values of B2-B8 (Fig.3 element 24 input address line B2-B7/A6-A0), respectively, for μ-law input. Now, returning back to Fig.3, at any instant period of time, there is only one PCM channel being selected and identified with respect to the particular B2-B7 values shown in Table 1 or 2 along with the control bits, P, M1, M0, C2, C1 and C0, and being converted from one of two different modulation standard (A-law or μ-law) to the other one of the two modulation standards (μ-law or A-law). Therefore, it is clear that Takahashi teaches a channel selector (Fig.2 element 23, Fig.3 signal B8-B2,

A6-A0, column 3 lines 44-50) for generating a channel select signal (Fig.3 signal B8-B2) for identifying one of said plurality of communication channels (Tables 1 and 2) in said system.

Takahashi discloses all of the subject matter as described in the above paragraph except for specifically teaching a plurality of mixers for selectively releasing and transmitting said input digital signal modulated by said one of said two different modulation standards and said converted input digital signal to the other one of said two different modulation standards by said codec means in response to said channel select signal.

However, by examining the disclosure of the instant application that the mixer discloses by the instant application is nothing but a data output buffer circuit controlled by an enable signal that can be integrated into a memory or ROM device.

Eagan et al. teaches a memory (Fig.1 element 30 and column 4 line 28) integrated with a data output buffer (Fig.1 element 38 and column 4 line 65 – column 5 line 15, and column 6 line 29-43) controlled by an enable signal (Fig.3 element SE or /SE) derived by Read/Write logic (Fig.1 element 35).

It is desirable to have a data output buffer integrated inside a memory in order to improve the time synchronization of the output data and reduce the size of the PCB. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include a data output buffer as taught

by Eagan et al. into Takahashi's read only memory (ROM) so as to improve the time synchronization of the output data and reduce the size of the PCB.

- With regard claim 2, Takahashi further discloses a first sub-codec means for converting said input digital signal modulated by said one of two different modulation standards received in said identified at least one channel of the multiple channels into an analog signal (Fig.4 2nd box A-law to μ-law conversion) in response to said channel select signal (Fig.3 elements 29, 33, 34 and Table 3), and

  a second sub-codec means for converting said converted analog signal by said first codec means into corresponding digital signals in accordance with the other of said two different modulation standards (Fig.4 4th box μ-law to A-law conversion) in response to said channel select signal (Fig.3 elements 29, 33, 34 and Table 3).

- With regard claim 4, Takahashi further discloses that channel select signal is generated in response to a frame sync signal, a clock signal, and a read address controlled by said clock signal for reading an output data or in response to each time slot (Fig.3 elements 24,29, 32-34, and column 2 line 62 – column 3 line 6, and column 5 lines 26-51).

- With regard claim 5, Takahashi further discloses wherein said channel select signal is synchronized with said at least one channel of the multiple channels containing said input digital signals modulated by said one of said two different modulation standards (Fig.3 elements 24,29, 32-34, signal B8-B2, A6-A0, and

column 2 line 62 – column 3 line 6 and column 3 lines 44-50). In column 2 line 62 – column 3 line 6, Takahashi discloses that the digital switch module 10 includes a digital encoding law conversion memory 24, which controls encoding law conversion between the A-law and the μ-law trunks 13 and 14. The digital switch module 10 performs time division switching, whereby data is switched from one of the trunks, e.g., 13, to the other trunk 14 in time slots. A control memory 29 controls the conversion performed by the encoding law conversion memory 24 within each time slot. It is clear that at each time slot there will be only one channel for digital encoding law conversion and the channel select signal is synchronized with said at least one channel of the multiple channels containing said input digital signals modulated by said one of said two different modulation standards.

- With regard claim 6, all limitation is contained in claim 1 and 2. The explanation of all the limitation is already addressed in the above paragraph.
- In regard claim 10, all limitation is contained in claim 4. The explanation of all the limitation is already addressed in the above paragraph.
- In regard claim 11, all limitation is contained in claim 5. The explanation of all the limitation is already addressed in the above paragraph.

Allowable Subject Matter

6. Claims 3, 7 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted M Wang
Examiner
Art Unit 2611

Ted M. Wang